IN THE CLAIMS:

1. (Currently Amended) A method of simulating an integrated circuit, the method including the steps of:

performing a timing analysis of the circuits included in the integrated circuit to ensure that they meet specified timing criteria;

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria; and

improving those circuits that fail the soft error analysis to improve their resistance to soft errors.

2. (Original) A method according to Claim 1, wherein the improving step includes the step of improving those circuits that fail the soft error analysis by either having an additional voltage source or altering the capacitance of the circuits.

3. (Original) A method according to Claim 1, wherein, for each of a defined set of circuits, the step of performing soft error analysis is done after the step of performing a timing analysis.

4. (Original) A method according to Claim 1, further comprising the step of, after the improving step, performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria.

5. (Original) A method according to Claim 4, further comprising the step of, after the step of performing a further timing analysis, performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria.

6. (Original) A method according to Claim 5, further comprising the step of further improving those circuits that fail the further soft error analysis to further improve their resistance to soft errors.

7. (Currently Amended) A method ~~according to Claim 6,~~ of stimulating an integrated circuit, the method including the steps of:

performing a timing analysis of the circuits included in the integrated circuit to ensure that they meet specified timing criteria;

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

after the improving step, performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria;

after the step of performing a further timing analysis, performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria;

further improving those circuits that fail the further soft error analysis to further improve their resistance to soft errors;

wherein the further improving step includes the step of further improving those circuits that fail the further soft error analysis using one of two defined procedures depending on whether the circuits pass or fail the further timing analysis.

8. (Original) A method according to Claim 7, wherein:

for those circuits that fail both the further timing analysis and the further soft error analysis, the step of further improving the circuits includes the step of increasing the voltage applied to the circuits; and

for those circuits that pass the further timing analysis and fail the further soft error analysis, the step of further improving the circuits includes the step of increasing the capacitance of the circuits.

9. (Currently Amended) A method according to Claim 6, of stimulating an integrated circuit, the method including the steps of:

performing a timing analysis of the circuits included in the integrated circuit to ensure that they meet specified timing criteria;

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

after the improving step, performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria;

after the step of performing a further timing analysis, performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria;

further improving those circuits that fail the further soft error analysis to further improve their resistance to soft errors; wherein:

a first set of circuits fail the further timing analysis and fail the further soft error analysis;

a second set of circuits pass the further timing analysis and fail the further soft error analysis;

the step of further improving those circuits that fail the further soft error analysis includes the steps of

i) using one of a first set of defined procedures to further improve the first set of circuits, and

ii) using one of a second set of defined procedures to further improve the second set of circuits.

10. (Currently Amended) A system for simulating an integrated circuit, the system including:

means for performing a timing analysis of the circuits included in the integrated circuit to ensure that they meet specified timing criteria;

means for performing soft error analysis of the circuits to determine whether they meet specified soft error criteria; and

means for improving those circuits that fail the soft error analysis to improve their resistance to soft errors.

11. (Original) A system according to Claim 10, wherein the improving mans includes means for improving those circuits that fail the soft error analysis by either having an additional voltage source or altering the capacitance of the circuits.

12. (Original) A system according to Claim 10, wherein, for each of a defined set of circuits, the soft error analysis is done after the timing analysis.

13. (Original) A system according to Claim 10, further comprising means for performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria.

14. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for simulating an integrated circuit, said method steps including:

performing a timing analysis of the circuits included in the integrated circuit to ensure that they meet specified timing criteria;

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria; and

improving those circuits that fail the soft error analysis to improve their resistance to soft errors.

15. (Original) A program storage device according to Claim 14, wherein the improving step includes the step of improving those circuits that fail the soft error analysis by either having an additional voltage source or altering the capacitance of the circuits.

16. (Original) A program storage device according to Claim 14, wherein said method steps further comprise the step of, after the improving step, performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria.

17. (Original) A program storage device according to Claim 16, wherein said method steps further comprise the step of, after the step of performing a further timing analysis, performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria.

18. (Original) A program storage device according to Claim 16, wherein said method steps further comprise the step of further improving those circuits that fail the further soft error analysis to further improve their resistance to soft errors.

19. (New) A method according to Claim 1, wherein the improving step includes the step of:

using a first defined procedure to improve the resistance to soft errors of those circuits that pass the timing analysis and fail the soft error analysis; and

using a second defined procedure to improve the resistance to soft errors of those circuits that fail the timing analysis and fail the soft error analysis.